VHDL for Combinational Circuits and Storage Elements

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**Introduction**

The purpose of this lab is to learn about the multiplexer, decoder, and encoder circuits. These circuits specialize in allowing specific paths or choosing specific paths given a certain input.

**Results**

Text

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**Figure 1:** VHDL code of 2:1 multiplexer

A screenshot of a computer

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**Figure 2:** Block Schematic Diagram of the implementation of 4:1 Mux using Figure 1 Mux SymbolChart, box and whisker chart

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**Figure 3:** Waveform of Figure 2

Text

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**Figure 4:** VHDL code of 2:4 decoder  
Diagram, schematic

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**Figure 5:** Block Schematic Diagram of the implementation of 3:8 Decoder using Figure 3 2:4 Decoder Symbol

A picture containing diagram

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**Figure 6:** Waveform of Figure 4

A picture containing graphical user interface

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**Figure 7:** VHDL code for encoder

**Analysis**

In Figure 1, VHDL code produces a symbol of a 2 to 1 multiplexer. This code was retrieved from the textbook Figure 6.28 and was properly formatted and fixed, so it’d compile and run properly. This symbol was later implemented into Figure 2 to create a 4 to 1 multiplexer. This circuit should produce relative to the input given a certain control value which is taken in by ‘s’. Further in Figure 3, the VHDL code can be observed which was taken from the textbook and fixed, so it’d compile and run properly. This code would produce a 2 to 4 decoder which then implemented into a 3 to 8 decoder as seen in Figure 4. This circuit should produce different output for each logic case produced by the input. In Figure 5, a set of VHDL code can be seen which would produce a 4 to 2 encoder circuit. This circuit functions as an encoder, outputting a certain set value based off the given input values.

It can be seen in Figure 3, the produced waveform given a set of input values produces the correct values that are expected for a mux. Similar with Figure 6, the provided signal for the 3 to 8 decoder circuit produces the correct output split into 2 output pins ‘y’ and ‘z’.